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| EXAMINER | |
|---|---|
| WALTER, CRAIG E | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/749,900 | KO ET AL. | |
| | Examiner | Art Unit | |
| | Craig E. Walter | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4 and 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Status of Claims*

1. Claims 1-4 and 6 are pending in the application.

Claims 1-4 and 6 have been amended.

Claim 5 has been canceled.

Claims 1-4 and 6 are rejected.

### *Response to Amendment*

2. Applicant's amendments and arguments filed on 15 May 2006 in response to the office action mailed on 23 February 2006 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

### *Claim Objections*

3. Claims 1-3 are objected to because of the following informalities:

As for claim 1, the word "in", as recited on line 17 of the claim should be omitted.

As for claim 3, the phrase "initialization selection signal" as recited in lines 8 and 13 should be changed "initialization enable signal" to establish antecedent basis for the phrase.

Claim 2 is objected to for further inheriting the deficiencies of claim 1.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-4, and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, the phrase "the logical cell block address in the row address" as recited in line 8 of the claim lacks antecedent basis, as no logical cell block address has been previously set forth as being contained "in the row address". Is this the same logical cell block address as recited in lines 3-4 of the claim?

As for claim 3, the phrase "selectively outputting one of the logical cell block address and an initialization signal to initialize corresponding unit tag tables" as recited in lines 9-10 renders the claim indefinite. The Examiner still cannot determine if Applicant intends to output one of the logical cell block addresses and an initialization signal, or outputting either one logical cell block address or an initialization signal to initialize corresponding unit tag tables. Additionally, the phrase "selectively outputting one of a local address to select one of M number of words lines" as recited in lines 14-15 renders the claim indefinite. The Examiner assumes Applicant intended to recite selecting one of a plurality of local addresses to output.

As for claim 4, the claim recites the step of performing said operation "by using the tag block". This limitation renders the claim indefinite, as one of ordinary skill in the art would be unable to ascertain how the block is being used to perform said operation. Likewise, there is insufficient antecedent basis for the limitation "the N number of unit tag tables" recited in line 9 as N number of unit tag tables is not previously set forth in the claim, or the claim from which it depends. Which among the N+1 unit tag tables are being claimed here?

As for claim 6, there is insufficient antecedent basis for the limitation "nullifying the N+1 number of unit tag tables" recited in line 6 of the claim as unit tag tables are not previously presented within the claim. Additionally, there is insufficient antecedent basis for the limitation "the N number of unit tag tables" recited in line 8, as N number of unit tag tables is not previously set forth in the claim, or the claim from which it depends. Which among the N+1 unit tag tables are being claimed here?

Claim 2 inherits the deficiencies of claim 1, therefore it too stands rejected under 35 U.S.C. 112.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jarboe, JR. et al. (US PG Publication 2004/0153793 A1) hereinafter Jarboe, in further view Yamaguchi et al., hereinafter Yamaguchi (US Patent 5,584,003).

As for claim 4, Examiner asserts that Jarboe in further view of Yamaguchi renders claim 4 obvious based of the Examiner's best understanding of the claim in light of the ambiguities set forth under section 4 of this correspondence. More specifically, Jarboe discusses initializing a tag block, and performing memory operations (i.e. read/write) based on the tag information – paragraph 0020, all lines. Yamaguchi teaches a plurality of tables used to store information on cell blocks (i.e. addresses), and further selecting the tables in order to address the cell blocks (see col. 3, lines 51 through col. 4, lines 15.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Jarboe to further include Yamaguchi's control system into his own system for testing embedded memory. By doing so, Jarboe would benefit by improving address conversion of the memory, thus resulting in higher processor performance as taught by Yamaguchi (col. 2, lines 37-47).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burger et al. (US Patent 6,557,080 B1) hereinafter Burger, in further view of Yamaguchi (US Patent 5,584,003).

As for claim 6, Burger teaches a method for a refresh operation of a semiconductor device including a cell area (Fig. 1, element 16) having N+1 number (in this example, 6) of unit cell blocks (element 20), each including M

number of word lines which respectively are coupled to a plurality of unit cells (elements 24) – col. 4, lines 34-47. Note since the specification defines M as any positive integer, the number of word lines can be *any* positive integer. Though the word lines are not illustrated in Fig. 1, word lines are inherently part of a cache memory. A tag block having N+1 (in this example, 6) number of unit tag blocks, each having M number of registers for sensing an update of data comprising (col. 4, line 53 through col. 5, line 6).

Burger additionally teaches the N number of unit cell blocks as corresponding to an address (Fig. 1, element 20 –blocks within the cache correspond to an unique addresses) and one unit cell block s added for accessing data with high speed (Burger specifically discusses access speed of memory as being an issue to overcome. The entire cache (N cell blocks + the 1 remaining) are specifically designed *for* storing accessing high speed data as recited in this claim – col. 1, lines 22-43).

Despite these teachings Burger fails to teach nullifying the N+1 number of unit tag tables, selecting the N+1 number of unit tag tables, and storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables.

Examiner asserts that Burger in further view of Yamaguchi renders claim 6 obvious based of the Examiner's best understanding of the claim in light of the ambiguities set forth under sections 4 of this correspondence (more specifically with respect to the rejections set forth under 112 2$^{nd}$ paragraph against these limitations). Yamaguchi teaches a plurality of tables used to store information on cell blocks (i.e.

addresses), and further selecting the tables in order to address the cell blocks (see col. 3, lines 51 through col. 4, lines 15. It would have been obvious to one of ordinary skill in the art at the time of the invention for Burger to further include Yamaguchi's control system into his own high-speed cache with dynamic control of sub-block fetching. By doing so, Burger would benefit by improving address conversion of the memory, thus resulting in higher processor performance as taught by Yamaguchi (col. 2, lines 37-47).

It is worthy to note that the "nullifying", "selecting", and "storing" limitations of this claim were identical to the limitations of cancelled claim 5, and presently amended claim 4. Applicant has not produced any arguments with respect to Yamaguchi's teachings of these three limitations in the Remarks section, hence the original rejection is maintained.

***Response to Arguments***

7. Applicant's arguments with respect to claim 4 have been considered but are not persuasive.

As for claim 4, Applicant has amended the claim to attempt to overcome rejections sets forth under §112, and to incorporate material canceled from claim 5. Applicant asserts that Jarboe fails to teach a method "[for] controlling a tag block for assigning a physical unit cell address based on a logical unit cell block". Examiner finds this augment not persuasive as this recitation is included in the preamble of the claims, and merely sets forth ~~was~~ what the method might be used *for* (emphasis added). Examiner asserts that the combined teachings of Jarboe and

Yamaguchi meet this recitation, as their combined teachings can be used *for* assigning a physical unit cell address based on a logical unit cell block. In summary, Examiner contends that appropriate patentable weight has been given to Applicant's recitation in the preamble as to what the system might be used *for* (i.e. assigning addresses to a unit cell block).

Applicant additionally asserts that Jarboe fails to teach initializing the tag blocks as including the three steps recited in this claims (i.e. the steps including "nullifying", "selecting", and "storing". Examiner however maintains that the original rejection asserted that Yamaguchi, not Jarboe teach these limitations. Since no specific arguments have been presented with respect to Yamaguchi's teachings, the rejection is maintained. Again art was applied to this claim based on the Examiner's best understanding based on the ambiguities set forth under section 4 of this correspondence.

Additionally, please note that Applicant mistakenly failed to indicate the added claimed subject matter incorporated into claim 4 (from canceled claim 5) via the use of appropriate markings (i.e. underlining).

8. Additional comments in response to Applicant's remarks and amendments are presented below:

With respect to claim 6, it is worthy to note that the "nullifying", "selecting", and "storing" limitations of this claim were identical to the limitations of cancelled claim 5, and presently amended claim 4. Applicant has not produced any arguments with respect to Yamaguchi's teachings of these three limitations in the

Remarks section, hence the original rejection is maintained based on the Examiner's best understanding based on the ambiguities set forth under section 4 of this correspondence.

The rejection of claim 4 under §112 found on page 5, lines 18-21 of the previous correspondence is maintained, as Applicant has neither amended the claim to overcome, nor presented an argument to traverse, the rejection.

The rejection of clam 5 under §112 found on page 6, line 21 through page 7, line 7 of the previous correspondence is applied to currently amended claim 4 as Applicant has neither amended the claim to overcome, nor presented an argument to traverse, the rejection of these limitations. The Examiner has withdrawn the rejection addressing the limitation "each different logical unit cell block".

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

7/6/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER